

WHAT IS CLAIMED IS:

- 1                   1.     A method for synthesizing a circuit representation into a new  
2 circuit representation having greater unateness, the method comprising:  
3                   (i) partitioning the circuit representation to obtain a representation of  
4 at least one sub-circuit;  
5                   (ii) recursively decomposing the representation of the at least one sub-  
6 circuit into a sum-of-products or product-of-sums representation having greater  
7 unateness than the representation of the at least one sub-circuit; and  
8                   (iii) merging the sum-of-products or product-of-sums representation  
9 into the circuit representation to form a new circuit representation.
- 1                   2.     The method of claim 1 additionally comprising repeating steps  
2 (i), (ii) and (iii) until a desired level of unateness for the new circuit representation  
3 has been achieved.
- 1                   3.     The method of claim 1 wherein the sum-of-products or  
2 product-of-sums representation selected for each decomposition is the representation  
3 having fewer binate variables.
- 1                   4.     The method of claim 1 additionally comprising merging  
2 common expressions of the sum-of-products or product-of-sums representations.
- 1                   5.     The method of claim 4 wherein algebraic division is  
2 implemented to merge common unate expressions of the sum-of-products or  
3 product-of-sums representation.
- 1                   6.     The method of claim 1 wherein the circuit is a digital circuit.
- 1                   7.     The method of claim 1 wherein the representation of the at  
2 least one sub-circuit is highly unate.

1                   8.     The method of claim 1 wherein a binary decision diagram is  
2 employed to recursively decompose the representation of the at least one sub-circuit  
3 into the sum-of-products or product-of-sums representation.

1                   9.     The method of claim 8 wherein the binary decision diagram  
2 is a zero-suppressed binary decision diagram.

1                   10.    A system for synthesizing a circuit representation into a new  
2 circuit representation having greater unateness, the system comprising a computing  
3 device configured to:

- 4                   (i) receive input defining the circuit representation;  
5                   (ii) partition the circuit representation to obtain a representation of  
6 at least one sub-circuit;  
7                   (iii) recursively decompose the representation of the at least one sub-  
8 circuit into a sum-of-products or product-of-sums representation having greater  
9 unateness than the representation of the at least one sub-circuit;  
10                  (iv) merge the sum-of-products or product-of-sums representation into  
11 the circuit representation to form the new circuit representation; and  
12                  (v) output the new circuit representation.

1                   11.    The system of claim 10 wherein the computing device is  
2 additionally configured to:  
3                   receive input defining a desired level of unateness for the new circuit  
4 representation; and  
5                   repeat steps (ii), (iii) and (iv) until the desired level of unateness is  
6 achieved.

1                   12.    The system of claim 10 wherein the computing device is  
2 additionally configured to, for each decomposition, select the sum-of-products or  
3 product-of-sums representation having fewer binate variables.

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1                   13.    The system of claim 10 wherein the computing device is  
2 additionally configured to merge common expressions of the sum-of-products or  
3 product-of-sums representations.

1                   14.    The system of claim 13 wherein the computing device is  
2 additionally configured to implement algebraic division to merge common  
3 expressions.

1                   15.    The system of claim 10 wherein the circuit is a digital circuit.

1                   16.    The system of claim 10 wherein the representation of the at  
2 least one sub-circuit is highly unate.

1                   17.    The system of claim 10 wherein the computing device is  
2 additionally configured to employ a binary decision diagram to recursively  
3 decompose the representation of the at least one sub-circuit into the sum-of-products  
4 or product-of-sums representation.

1                   18.    The system of claim 17 wherein the binary decision diagram  
2 is a zero-suppressed binary decision diagram.

1                   19.    The system of claim 10 wherein the circuit representation and  
2 the new circuit representation are input and output in a hardware description  
3 language.

1                   20.    A system for synthesizing a circuit representation into a new  
2 circuit representation having greater unateness, the system comprising:

3                   (i) a means for receiving input defining the circuit representation;

4                   (ii) a means for partitioning the circuit representation to obtain a  
5 representation of at least one sub-circuit;

6                   (iii) a means for recursively decomposing the representation of the  
7 at least one sub-circuit into a sum-of-products or product-of-sums representation  
8 having greater unateness than the representation of the at least one sub-circuit;

- 9 (iv) a means for merging the sum-of-products or product-of-sums  
10 representation into the circuit representation to form the new circuit representation;  
11 and  
12 (v) a means for outputting the new circuit representation.

1 21. The system of claim 20 additionally comprising:  
2 a means for receiving input defining a desired level of unateness for  
3 the new circuit representation; and  
4 a means for repeating steps (ii), (iii) and (iv) until the desired level  
5 of unateness is achieved.

1 22. The system of claim 20 additionally comprising a means for  
2 selecting, for each decomposition, the sum-of-products or product-of-sums  
3 representation having fewer binate variables.

1 23. The system of claim 20 additionally comprising a means for  
2 merging common expressions of the sum-of-products or product-of-sums  
3 representations.

1 24. The system of claim 20 additionally comprising a means for  
2 implementing algebraic division to merge common expressions.

1 25. The system of claim 20 additionally comprising a means for  
2 partitioning the circuit representation such that the representation of the at least one  
3 sub-circuit is highly unate.

1 26. The system of claim 20 additionally comprising a means for  
2 employing a binary decision diagram to recursively decompose the representation  
3 of the at least one sub-circuit into the sum-of-products or product-of-sums  
4 representation.

1 27. The system of claim 26 wherein the binary decision diagram  
2 is a zero-suppressed binary decision diagram.

1                   28.    The system of claim 20 wherein the circuit representation and  
2   the new circuit representation are input and output in a hardware description  
3   language.

1                   29.    A computer-readable storage medium containing computer  
2   executable code for instructing one or more computers to:  
3                   (i) receive input defining a circuit representation;  
4                   (ii) partition the circuit representation to obtain a representation of  
5   at least one sub-circuit;  
6                   (iii) recursively decompose the representation of the at least one sub-  
7   circuit into a sum-of-products or product-of-sums representation having greater  
8   unateness than the representation of the at least one sub-circuit;  
9                   (iv) merge the sum-of-products or product-of-sums representation into  
10   the circuit representation to form a new circuit representation; and  
11                   (v) output the new circuit representation.

1                   30.    The computer-readable storage medium of claim 29 wherein  
2   the computer executable code additionally instructs the computer(s) to:  
3                   receive input defining a desired level of unateness for the new circuit  
4   representation; and  
5                   repeat steps (ii), (iii) and (iv) until the desired level of unateness is  
6   achieved.

1                   31.    The computer-readable storage medium of claim 29 wherein  
2   the computer executable code additionally instructs the computer(s) to, for each  
3   decomposition, select the sum-of-products or product-of-sums representation having  
4   fewer binate variables.

1                   32.    The computer-readable storage medium of claim 29 wherein  
2   the computer executable code additionally instructs the computer(s) to merge  
3   common expressions of the sum-of-products or product-of-sums representations.

1                    38.     The computer-readable storage medium of claim 29 wherein  
2     the circuit representation and the new circuit representation are input and output in  
3     a hardware description language.

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